

Fig.2

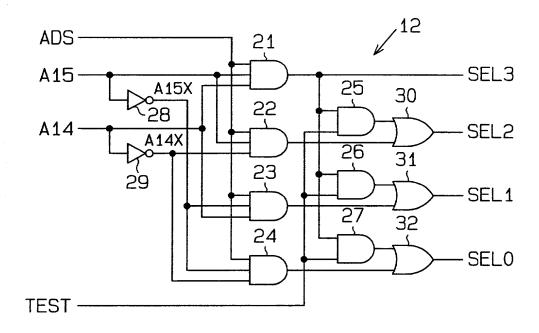


Fig.3

Upper Address Decode Signal	A15	A14	TEST	SEL3	SEL2	SEL1	SEL0
1	0	0	0	0	0	0	1
1	0	1	0	0	0	1	0
1	1	0	0	0	1.	0	0
1	1	1	0	1	0	0	0
1	0	0	1	0	0	0	1
1	0	1	1	0	0	1	0
1	1	0	1	0	1	0	0
1	1	1	1	1	1	1	1
0	Х	Χ	Х	0	0	0	0

Fig.4

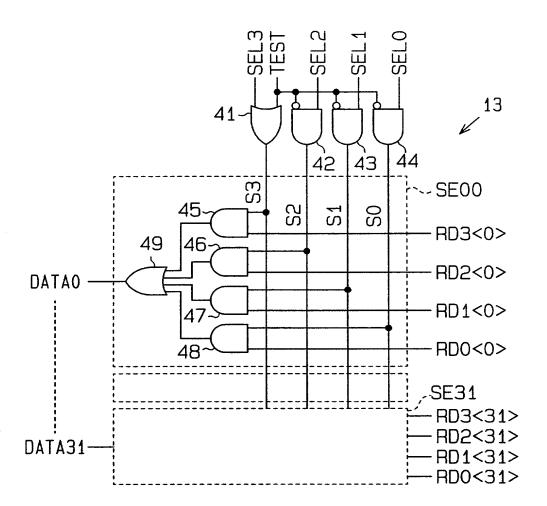


Fig.5

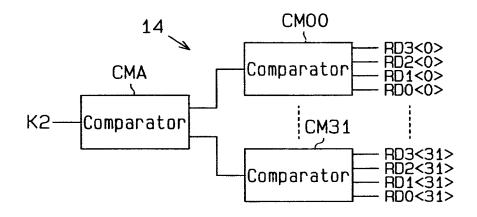


Fig.6

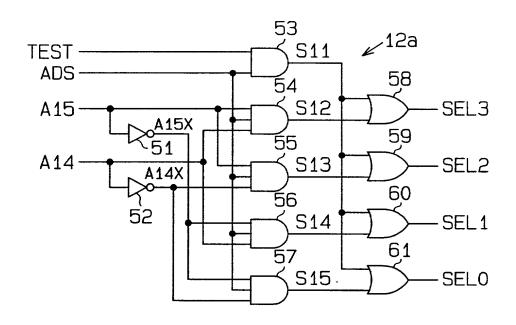


Fig.7

Upper Address Decode Signal	A15	A14	TEST	SEL3	SEL2	SEL1	SEL0
1	0	0	0	0	0	0	1
1	0	1	0	0	0	1	0
1	1	0	0	0	1	0	0
1	1	1	0	1	0	0	0
1	Χ	Χ	1	1	1	1	1
0	Χ	Х	X	0	0	0	0

Fig.8

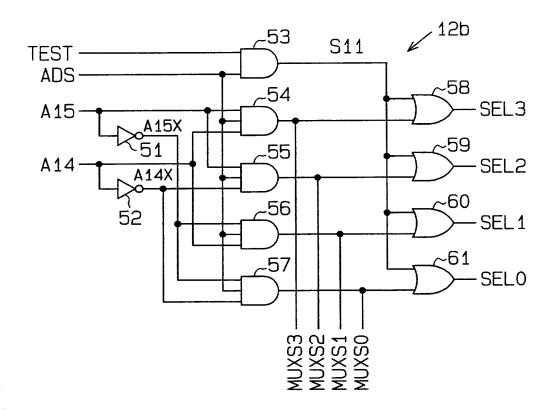
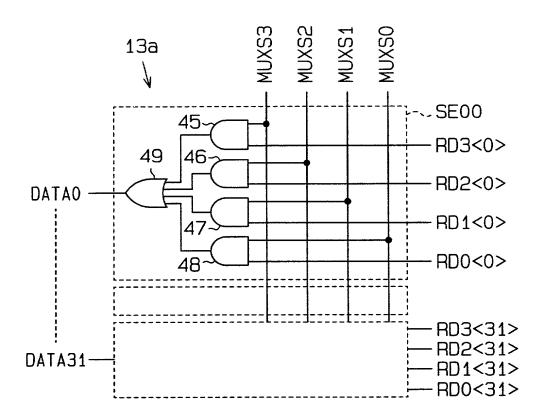


Fig.9

Upper Address Decode Signal	A15	A14	TEST	SEL3	SEL2	SEL1	SEL0
1	0	0	0	0	0	0	1
1	0	1	0	0	0	1	0
1	1	0	0	0	1	0	0
1	1	1	0	1	0	0	0
1	Х	Х	1	1	1	1	1
0	Х	Χ	Х	0	0	0	0

Fig.10



RAM3 BAM2 BAMO RAM1 Comparator 1∕72 SEL1 SEL2 SEL3 ~ 12 Fig.11 Address Decoder TEST 13~ DATA 18 15 SP X 1

·70

Fig.12

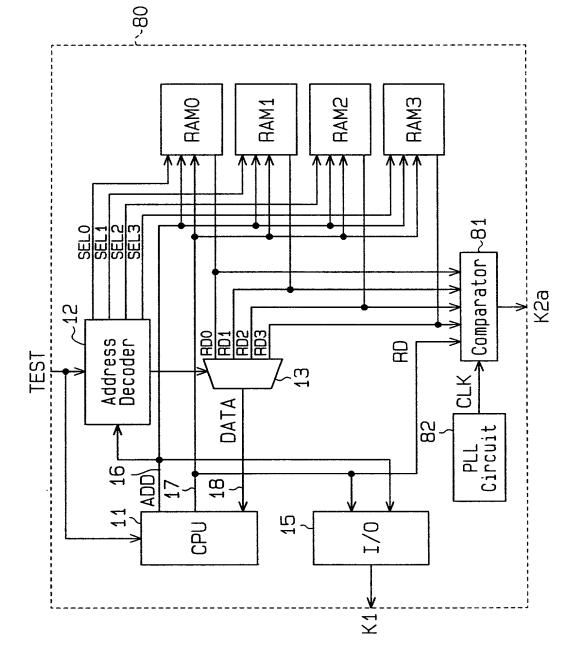


Fig.13

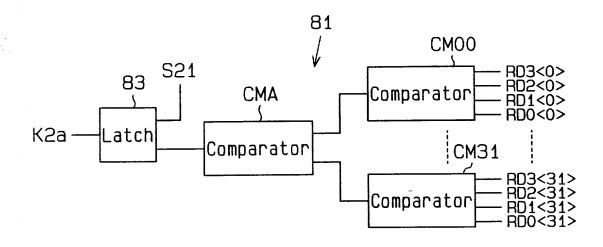
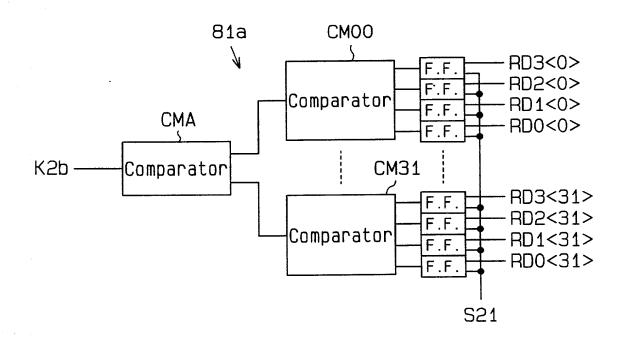


Fig.14



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Fig.15

